

INFORMATION DISCLOSURE STATEMENT BY APPLICANTS PTO-1449	Attorney Docket No. 2885/93	Serial No. 10/523,764
	Applicant(s) VORBACH et al.	
	Filing Date August 2, 2005	Group Art Unit 2185

U.S. PATENT DOCUMENTS

EXAMINER'S INITIALS	PATENT/ PUBLICATION NUMBER	PATENT/PUBLICATION DATE	NAME	CLASS	SUBCLASS	FILING DATE
	4,151,611	April 24, 1979	Sugawara et al.			
	5,036,493	July 30, 1991	Nielsen			
	5,568,624	October 22, 1996	Sites et al.			
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	6,078,736	June 20, 2000	Guccione			
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	6,725,334	April 20, 2004	Barroso et al.			
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	2002/0099759	July 25, 2002	Gootherts			
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FOREIGN PATENT DOCUMENTS

EXAMINER'S INITIALS	DOCUMENT NUMBER	DATE	COUNTRY	CLASS	SUBCLASS	TRANSLATION	
						YES	NO

OTHER DOCUMENTS

EXAMINER'S INITIALS	AUTHOR, TITLE, DATE, PERTINENT PAGES, ETC.
	Culler, D.E; Singh, J.P., "Parallel Computer Architecture," Page 17, 1999, Morgan Kaufmann, San Francisco, CA USA, XP002477559.
	Short, Kenneth L., <u>Microprocessors and Programmed Logic</u> , Prentice Hall, Inc., New Jersey 1981, p. 34.
	Webster's Ninth New Collegiate Dictionary, Merriam-Webster, Inc., 1990, page 332 (definition of "dedicated").
EXAMINER	DATE CONSIDERED
EXAMINER: Initial if citation considered, whether or not citation is in conformance with M.P.E.P. 609; draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant.	